What is claimed is:

1. A hardware/software system for storing and downloading a data packet comprising:

a first configuration register for storing an offset value representing an amount of memory preceding the first line of the data packet to be stored;

a second configuration register for storing an offset value representing an amount of memory following the end of the last line of the data packet to be stored; and

a mechanism for allocating a portion of memory for storage of data packet;

characterized in that the offsets indicated by the first and second configuration registers are added to size of the data packet to be stored, resulting in a new size for memory allocation.

2. The hardware/software system of claim 1 implemented within a data packet router connected to a data packet network.

3. The hardware/software system of claim 2 wherein the data packet network is the Internet network.

4. The hardware/software system of claim 1 wherein the hardware accesses the first and second configuration registers, computes the required size of memory allocation, and allocates the memory for packet storage.

5. The hardware/software system of claim 1 wherein the software accesses the first and second registers, computes the required size of memory allocation, and allocates the memory for packet storage.

6. The hardware/software system of claim 1 wherein the hardware accesses the first and second registers and passes the values to the software to complete the computation and allocation of the memory to store the data packet.

7. The hardware/software system of claim 1 further comprising one or more additional sets of registers for storing memory values applicable and specific to data packet types, each set associated with the type of data packet other than a type associated with the first and second registers.

8. The hardware/software system of claim 1 wherein the first and second registers are configurable during a boot operation of the system.

9. The hardware/software system of claim 7 wherein the one or more additional sets of registers are configurable during a boot operation of the system.

10. The hardware/software system of claim 1 wherein change values for the first and second registers may be entered into the registers during operation of the system.

11. The hardware/software system of claim 7 wherein change values for the one or more additional sets of registers may be entered into the registers during operation of the system.

12. The hardware/software system of claim 1 wherein any changes in packet size during processing are tracked, and the first configuration register is

consulted before download of the packet, to determine the actual starting point of the processed packet in memory.

13. A method for storing and downloading a data packet, comprising the steps of:

(a) providing an offset value in a first configuration register representing an amount of memory preceding the first line of the data packet to be stored;

(b) providing an offset value in a second configuration register representing an amount of memory following the last line of the data packet to be stored

(c) upon arrival of a data packet to be stored, accessing the first and second configuration registers for the offset values;

(d) summing the acquired values with the original size of the data packet to be stored; and

(e) allocating memory for the packet according to the sum in step (d).

14. The method of claim 13 implemented within a data packet router connected to a data packet network.

15. The method of claim 14 wherein the data packet network is the Internet network.

16 The method of claim 13 wherein, in steps (a) and (b) the registers are accessible by hardware responsible for storing the data packet.

17. The method of claim 13 wherein in steps (a) and (b) the values are configured into each register during a boot operation of a host system.

18. The method of claim 13 wherein in step (c) access is performed by hardware;

19. The method of claim 13 wherein in step (c) access is performed by software.

20. The method of claim 13 wherein a step is added between steps (c) and (d) for passing the values to software.

21. The method of claim 13 wherein steps (c) through (e) are performed entirely by hardware.

22. The method of claim 13 wherein step (c) is performed by hardware and steps (d) and (e) are performed by software.

23. The method of claim 13 wherein in steps (a) and (b) the registers are configured during boot operation.

24. The method of claim 13 wherein in step (e) the memory is local packet memory that is hardware controlled.

25. The method of claim 13 wherein in steps (a) and (b) there are a plurality of register sets, each set dedicated to a different type of data packet.

26. The method of claim 13 further comprising steps for tracking growth and shrink of a data packet during processing, and for consulting the first configuration register after processing and before download to determine the actual starting point of the processed packet in memory.